國立台灣科技大學 114學年 第2學期　課程大綱

Spring 2026 NTUST Course Outline

授課教師：林敬舜

Instructor:Ching-Shun Lin

課程名稱：數位邏輯設計

Course Title：Digital Logic Design

2026/11/3

課程代號： ET3305301 Course Code 學分數： 3 Credits	必選修：必修/半學年 Required/Electve:Required/Half Yr. 先修課程： Prerequisites
節次教室： Time/Location	T4(IB-308) W6(IB-308) W7(IB-308)
專業核心能力： Core Professional Competencies	
課程網址： Course Website	https://www.et.ntust.edu.tw/et/faculty.php?user=chingshl
課程宗旨： Course Objectives	This course introduces students to the basic concepts of digital systems, including analysis and design. Both combinational and sequential logic will be covered in the lectures. Students will gain experience with several levels of digital systems, from simple logic circuits to programmable logic devices and hardware description language. Additionally, we will pay particular attention to design principles and techniques, timing analysis, and finite state machines. The concepts covered in this class are needed in other courses in electrical and computer engineering.
課程大綱： Outline of Lectures	• Binary number systems, number representations, and codes • Boolean algebra Boolean functions • Logic gates and circuits • Logic simplification using Boolean algebra and Karnaugh maps • Combinational logic design and building blocks • Synchronous sequential logic design and state machines • Latches, flip-flops, registers and counters • Programmable logic • Memory basic • Verilog programming
授課方式： Method of Instruction	講授 Lecture：70% 分組討論 Group discussion：10% 案例研討 Case study：10% 操做練習 Practical exercises：10% 講授 Lecture：Some supplementary materials will be handed out in the lecture.%
教科書： Textbooks	1. M. Moris Mano and Michael D. Ciletti, Digital Design, Global Ed., Pearson, 2019. 2. Ming-Bo Lin, Digital Logic Design: With An Introduction to Verilog HDL, W. W. Norton, 2016. 3. Ming-Bo Lin, Digital Systems Design and Practice: Using Verilog HDL and FPGAs, CreateSpace Independent Publishing Platform, 2015. 4. Ming-Bo Lin, A Tutorial on FPGA-Based System Design Using Verilog HDL: Intel/Altera Quartus Version: Part I: An Entry-Level Tutorial, W. W. Norton, 2018.

參考書目： References	1. David Harris and Sarah Harris, Digital Design and Computer Architecture, 2nd Ed., Morgan Kaufmann, 2012. 2. Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with Verilog Design, 3rd Ed., McGraw Hill, 2013. 3. Frank Vahid, Digital Design with RTL Design, VHDL, and Verilog, 2nd Ed., John Wiley & Sons Inc, 2010.
修課須知： Notice	Teaching assistant is available.
評量方式： Grading	Midterm: 40 % Final exam: 40 %, Attendance and Participation: 10 % Quiz: 10%
備註說明： Notes	Tips for success in this class: • Familiarity with programming, such as the C language, is a plus. • Don’t miss class. • Read in advance. • Start homework early. • Don’t ignore the homework, and quizzes. • Ask questions. • Don’t arrive late for class.