國立台灣科技大學 114學年 第2學期　課程大綱

Spring 2026 NTUST Course Outline

授課教師：沈中安

Instructor:Chung-An Shen

課程名稱：數位邏輯設計實習

Course Title：Lab. of Digital Logic Design

2026/11/3

課程代號：ET3806302 Course Code 學分數：1 Credits	必選修：必修/半學年 Required/Electve:Required/Half Yr. 先修課程： Prerequisites
節次教室：W7(T2-511) W8(T2-511) W9(T2-511) Time/Location	
專業核心能力： Core Professional Competencies	
課程網址： Course Website	
課程宗旨： Course Objectives	1.示波器及邏輯分析儀之操作與使用 2.PLD發展系統之操作與使用 3.Verilog HDL模擬器之操作與使用 4.Code Converter、Adder-subtractor、Counter及SRAM等數位電路之實作 5.Code Converter、Adder-subtractor、Counter及SRAM等數位電路之Verilog HDL模擬 6.Code Converter、Adder-subtractor、Counter、SRAM及Binary Multiplier等數位電路之PLD設計 1.Introduction to TTL series IC and basic electronic devices. 2.Use basic equipments for digital design: Oscilloscope, Function generator, Multi-meter, Logic Analyzer and Power supply etc..) 3.Use and introduction to basic tools for digital design: MAX+PLUS II, Quartus II, KeilC and ModelSim etc..) 4.Using ABEL to design digital circuit application for PALs.) 5.Using Verilog HDL to design digital circuit application for CPLD/FPGA.) 6.Using Microcontroller to design digital circuit application.)
課程大綱： Outline of Lectures	1.示波器及邏輯分析儀之操作與使用 2.PLD發展系統之操作與使用 3.Verilog HDL模擬器之操作與使用 4.Code Converter、Adder-subtractor、Counter及SRAM等數位電路之實作 5.Code Converter、Adder-subtractor、Counter及SRAM等數位電路之Verilog HDL模擬 6.Code Converter、Adder-subtractor、Counter、SRAM及Binary Multiplier等數位電路之PLD設計 1.Introduction to TTL series IC and basic electronic devices. 2.Use basic equipments for digital design: Oscilloscope, Function generator, Multi-meter, Logic Analyzer and Power supply etc..) 3.Use and introduction to basic tools for digital design: MAX+PLUS II, Quartus II, KeilC and ModelSim etc..) 4.Using ABEL to design digital circuit application for PALs.) 5.Using Verilog HDL to design digital circuit application for CPLD/FPGA.) 6.Using Microcontroller to design digital circuit application.)

授課方式： Method of Instruction	講授 Lecture：50% 分組討論 Group discussion：0% 案例研討 Case study：0% 操做練習 Practical exercises：50% 講授 Lecture：%
教科書： Textbooks	Digital Design with An Introduction to the Verilog HDL, VHDL, and SystemVerilog 6th edition, by M. Mano and Michael Ciletti, Pearson, 2018.
參考書目： References	
修課須知： Notice	
評量方式： Grading	Lab Exercises: 30% Midterm Exam: 30% Final Exam: 40%
備註說明： Notes	