國立台灣科技大學 114學年 第2學期　課程大綱

Spring 2026 NTUST Course Outline

授課教師：林銘波

Instructor:Lin, Ming-Bo

課程名稱：超大型積體電路設計

Course Title：VLSI Systems Design

2026/11/3

課程代號：ET5302701 Course Code 學分數：3 Credits	必選修：選修/半學年 Required/Electve:Elective/Half Yr. 先修課程： Prerequisites
節次教室：R2(IB-401) R3(IB-401) R4(IB-401) Time/Location	
專業核心能力： Core Professional Competencies	
課程網址： Course Website	
課程宗旨： Course Objectives	The objective of this course is to familiarize the student with the process of implementing a digital system as a full-custom integrated circuit. Upon completion, the student will be able to perform basic VLSI design from circuit concept to mask layout and simulation. To reach this, topics of this course include standard CMOS logic design, device fabrication, mask layout, introductory MOSFET physics, hierarchical IC design, and circuit simulation. Students will design, simulate, and do mask-level layout of a circuit using a modern CMOS process.
課程大綱： Outline of Lectures	1. Introduction to CMOS circuits (Chapter 1): MOS switches, CMOS fabrication and layout, and ratioless logic design. 2. MOS transistor theory (Chapter 2): I-V characteristics, C-V characteristics, nonideal I-V characteristics, and DC transfer characteristics. 3. Transient response (Chapter 4): Resistance estimation, capacitance estimation, switch-level delay models, power dissipation, design margining, sizing routing conductors, and yield. 4. Power (Chapter 5): Power and energy, dynamic power, static power, clock gating, and power gating. 5. Interconnect (Chapter 6): Wire geometry, wire resistance, wire capacitance, crosstalk, wire engineering, and repeater design. 6. Combinational logic design (Chapter 9): Bubble pushing, compound gates, logical effort example, input ordering, asymmetric gates, skewed gates,and best P/N ratio. 7. Sequential logic design (Chapter 10): Sequencing, sequencing element design, max and min-delay, clock skew, time borrowing, and two-phase clocking. 8. Adders (Chapter 11): Single-bit addition, carry-ripple adder, carry-skip adder, carrylookahead adder, carry-select adder, carry-increment adder, and tree adder. 9. Datapath function units (Chapter 11): Comparators, shifters, multi-input adders, and multipliers.
授課方式： Method of Instruction	講授 Lecture：100% 分組討論 Group discussion：0% 案例研討 Case study：0% 操做練習 Practical exercises：0%

	講授 Lecture：%
教科書： Textbooks	1. Neil H. E. Weste and David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed., New-York: Pearson Education, Inc., 2010. (ISBN-13: 978-0321547743) (International student edition: Integrated Circuit Design)
參考書目： References	1. R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, 2nd ed., IEEE/Wiley Interscience, 2005. 2. M. Rabaey Anantha Chandrakasan, and Borivoje Nikoli\'{c}, Digital Integrated Circuits: A Design Perspective, 2nd ed., Upper Saddle River, N. J.: Prentice-Hall, 2003. (ISBN-13: 978-0130909961)
修課須知： Notice	
評量方式： Grading	Homework: 40 pts; midterm exam: 30 pts; final exam: 30 pts.
備註說明： Notes	必須熟悉『數位邏輯設計』與大學「電子學」或『電子電路』。此外，『基本電路原理』也是必須的。 外校生請注意：因為需要使用工作站與TSRI提供的CAD軟體與製程完成作業，本課程不接受校際選課。